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| BLUEsat – UNSW Student Satellite Project -  Document BLUE.2011.1.0 |
| BLUEsat Primer |
| An introduction to the BLUEsat Student Satellite Project |
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| 9/24/2011 |

# Introduction

The purpose of this report is to consolidate the design of BLUEsat into a single document. The intention is that, by reading this particular report, the reader will be able to gain an overview of the nature of the BLUEsat project, its mission, project management philosophy and a brief technical overview of the design of the satellite itself.

Whilst this report contains some amount of technical detail regarding the design of the satellite, it is not intended to be a fully detailed technical master file. The rationale and overall design of each sub-system will be described such that the reader understands the nature of the satellite itself and how each system is related to each other. For a fully detailed technical report regarding the design of the satellite and current development progress, please consult document BLUE.2011.2.0 – BLUEsat Technical Design Report.

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# Project Background

# Project Management and SCRUM

# Satellite System Overview

BLUEsat’s intended purpose is to service the Amateur Radio community whilst being a vehicle for experimental payloads. That is, the satellite is to assist in communications between members of the Amateur Radio Community worldwide, whilst also allowing simple payloads to conduct experiments in space.

To that end, the satellite is physically designed much like other Amateur Radio Microsatellites - with much inspiration taken from ECHOsat (AO-51). The satellite is composed of trays in which will contain communications peripherals and the processing units which are responsible for the (relatively) autonomous operation of the satellite.

## Specifications

In order to function as a useful Amateur Radio Satellite, the satellite needs to be able to do the following (listed in increasing complexity but decreasing criticality)

1. Function as an Analogue Repeater
2. Function as a Digital Repeater
3. Be able to store and forward Data (PACsat)
4. Be able to control and process feedback from third party payload units via a generic serial interface

On top of this, the satellite needs to survive autonomously in Low-Earth Orbit (at an altitude of approximately 750km). This means that that along with the above functionality, the satellite must

1. Be able to power itself
2. Survive in a Vacuum
3. Survive the Radiation in a Space Environment
4. Be able to evaluate its own state

## System Design

The satellite itself is split into two main systems, each with its own central processing unit - the Payload Systems and the Critical Systems. Figure 6.1 illustrates the basic system overview and interconnectivity between systems within the satellite.

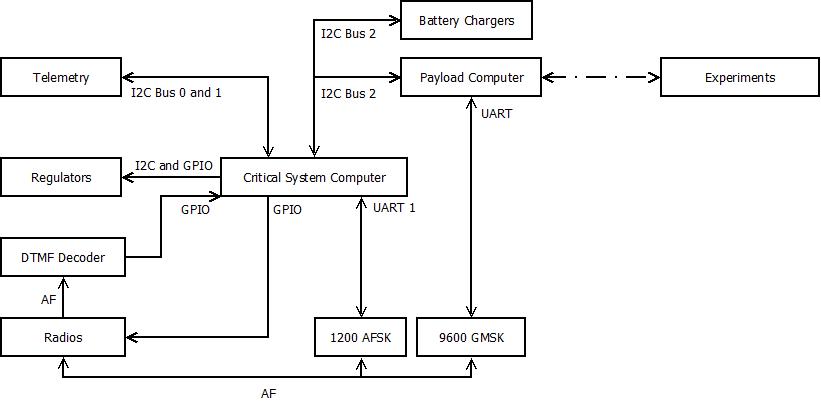


Figure 6.1 – Satellite Systems Overview

The Critical Systems deal with the basic functioning and survival of the satellite, as well as performing basic Analogue repeating. Critical Systems is responsible for powering the different electrical systems, monitoring the health of the satellite and maintaining basic communications with Earth. To that end, the Critical Systems is composed of

* The Critical Systems Computer (CSC)
* Telemetry System
* Communications System
  + Radio Transmitter and Receiver
  + 1200 baud AFSK Modems
* Power Distribution System
* Solar Array and Battery Charging System,

The Payload system consists of the Payload Computer and the experimental Payloads themselves. The Payload computer is to act as an interface between the Satellite’s Payloads and the Critical systems. The Payload computer also provides a separate modem (the 9600 baud GMSK modem) to allow for higher speed communications with the Groundstation.

The Payload system was made distinct from the Critical Systems to allow for greater modularity in the overall design of the satellite. To this end, integration of payloads will not greatly affect the design of the critical systems of the satellite.

## Mechanical Structure

*Relevant Drawings:*

|  |  |
| --- | --- |
| MECH0008 | Tray 0: Baseplate |
| MECH0009 | Tray 1: Transmitters |
| MECH0010 | Tray 2: Flight Computer |
| MECH0011 | Tray 3: Batteries |
| MECH0012 | Tray 4: Power Control |
| MECH0013 | Tray 5: Receivers |
| MECH0014 | Transmitter Housing |
| MECH0015 | Receiver Housing |

The Satellite’s Mechanical design is based off of other similarly sized Amateur Radio Microsatellites, with particular inspiration taken from ECHOsat (AO-51). The satellite is composed of five square trays stacked vertically to create a 250x250x250mm cube with a Solar Panel on each of the 6 sides.

The trays will contain the electronic circuitry of the satellite. There are connectors attached to the backplane of the satellite in order to allow for connections between trays. The trays (from top to bottom) are assigned electronics as follows (referencing Figure 6.2)

* Tray 5 - Radio Receiver and Hybrid Coupler
* Tray 4 - Payload Computer and Payload Systems
* Tray 3 - Batteries
* Tray 2 - Critical Systems and Power Systems
* Tray 1 - Radio Transmitter and Hybrid Coupler

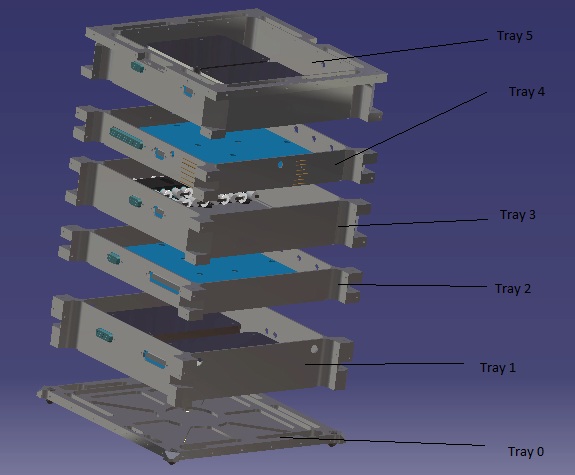


Figure 6.2 - Exploded view of the satellite tray system

Trays 5 and 1 have specialised mounting holes and covers in order to attach and shield the Radio units. Trays 4 and 2 are designed to maximise the amount of surface area available for printed circuit boards. Tray 3 is designed to allow for mounting of two battery packs that is to make up the battery array.

Once assembled, the trays allow for attachment of flat panels on each side, onto which the Solar Arrays will be mounted. The top and bottom panels will have allowance for Antennae footholds for radio transmission.

Detailed drawings and design rationales can be found in document BLUE.2011.2.0 – BLUEsat Technical Design Report.

## Communications

*Relevant Drawings:*

|  |  |
| --- | --- |
| *COMS0001* | *Beacon* |
| *COMS0002* | *AFSK Modem* |
| *COMS0003* | *DTMF Reciever* |
| *COMS0004* | *Switching Circuit* |
| *COMS0005* | *Comms Test Board* |

BLUEsat will communicate with Earth via VHF radio transmitters and UHF radio receivers. Digital data from the Critical Systems Computer and Payload Computer will be modulated by AFSK (Audio Frequency Shift Keying) and GMSK (Gaussian-Minimum Shift-Keying) modems, respectively, for transmission or reception by the radios.

Each of the above communication devices are duplicated for sake of redundancy. In order to manage communication lines and communication times, the critical systems compute controls a central switching circuit which routes communication lines based upon current priority. The communications array is connected according to Figure 6.3

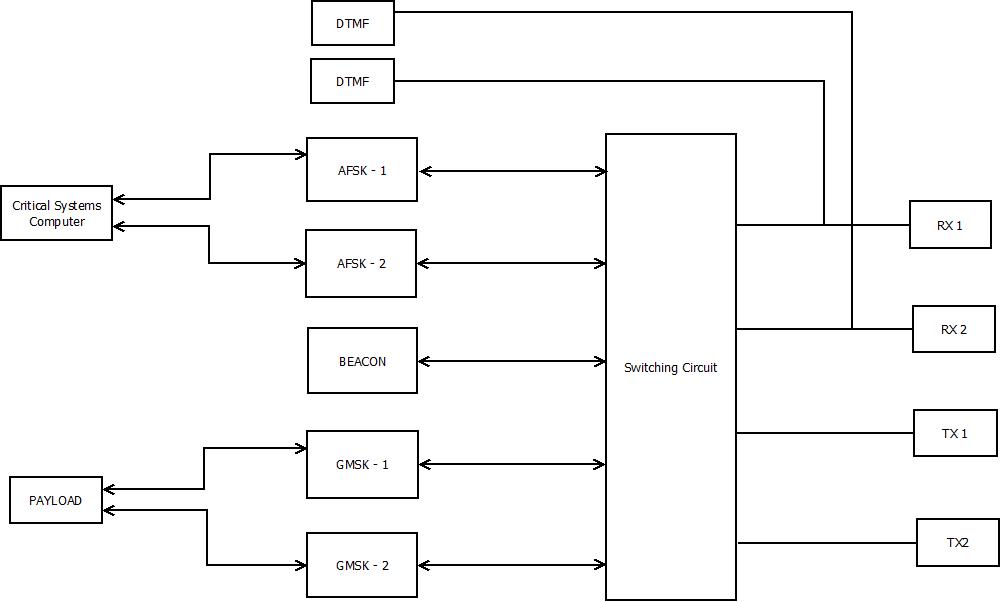


Figure 6.3 - Communications Layout

In addition to this the satellite will also process commands in the form of nine digit numbers, transmitted in DTMF (Dual-Tone Multi-Frequency) form. These commands will be decoded by a DTMF decoder for processing by the Critical Systems computer. The DTMF decoders bypass the switching circuit and are directly connected to each of the Radio Receivers (illustrated in XXXX).

The DTMF circuits are designed such that they will be constantly ‘listening’ for commands, and will alert the Critical Systems Computer when a valid command is received.

### DTMF

## Critical Systems Computer

*Relevant Drawings:*

|  |  |
| --- | --- |
| *CRSC0001* | *Critical System Computer - Top Level* |
| *CRSC0002* | *Critical System Computer - Microcontroller* |
| *CRSC0003* | *Critical System Computer - Memory* |
| *CRSC0004* | *Critical System Computer - Serial* |
| *CRSC0005* | *Critical System Computer - Power* |

The critical systems on the satellite (being the Communications, Telemetry and Power systems) will be controlled via a central micro-controller and memory system complete with a multi-threaded Operating System. This central controller is called the Critical Systems Computer. This system is to be distinct from the Payload Computer, whose responsibilities lie solely in interfacing with BLUEsat’s payloads.

The Critical Systems Computer will directly perform the following tasks

* Power Systems
  + Voltage Regulator Control
  + Battery Charge Regulator Control
* Telemetry data request and storage
* Communication
  + RX and TX Radio control
    - Power regulation
    - Line switching
  + AFSK (low speed) data transmission

The critical systems computer will run according to commands received from earth via transmission of nine digit codes transmitted in Dual Tone Multi Frequency (DTMF) format.

### LPC2468 Microcontroller

The microcontroller central to the design of the Critical Systems Computer is the ARM7 LPC2468 manufactured by NXP Semiconductors. Relevant circuit designs can be found in the CRSC family of drawings. The microcontroller was chosen for

* UNSW Undergraduate familiarity with the ARM7 family of microprocessors
  + Providing undergraduate engineers with an accessible and easy environment in which to develop
* The External Memory Controller
  + Simplifying interfacing with the CSC and the external memory needed to store telemetry and state data.
* The number of communication lines available
  + Three I2C enabled ports and Three UART ports
  + I2C is used on the satellite for communication with all of the Telemetry, Payload and power systems, whilst UART is used for both the 1200baud modems and for terminal debugging.
* The number of input/output ports available.
  + Required for switching of power regulation for each electrical subsystem in the satellite.

Currently, all hardware and software prototyping has occurred on a LPC2119 development board. This board (dubbed the “JTAG Board”) contains an LPC2119 ARM7 microcontroller. This board is both much cheaper and less feature heavy than the LPC2468 board, but contains the same architecture processor and contains a similar (if more lightweight) feature set. For these reasons, the LPC2119 is the ideal development tool for prototyping of all the satellite’s peripherals.

### FreeRTOS

On this microcontroller, BLUEsat will run a distribution of FreeRTOS (Free Real-Time Operating System), modified for the specific operational needs of the satellite.

This Operating System was chosen as it was open source project, provided a stable scheduler in a small footprint and has an active NXP ARM support.

The CSC OS is organized in the following fashion (Figure 6.4: CSC OS Structure)

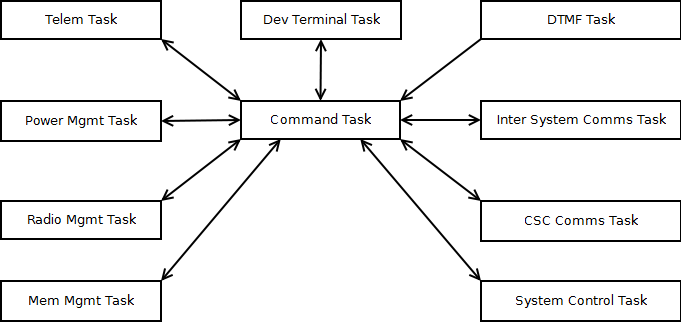


Figure 6.4: CSC OS Structure

Within the operating system, drivers and applications are intended to be run in order to control the critical systems of the satellite according to pre-defined constraints. Each task illustrated in Figure 6.4: CSC OS Structure calls applications relevant to the responsibilities defined below in Table 6.1: CSC Task responsibilities

Table .1: CSC Task responsibilities

|  |  |
| --- | --- |
| Task Name | Description |
| **Command Task** | High Priority message switching task to allow inter process communication. |
| **System Control Task** | Manage operation modes and effect commands from the Ground Station. |
| **Telemetry Task** | Gathers telemetry data, archives old data and packages up responses to be sent to the Ground Station. |
| **Power Management Task** | Manage system power usage based on operation modes and available power by turning on and off subsystems via the regulators. |
| **Radio Management Task** | Controls which devices have access to the radios. |
| **Memory Management Task** | Provide persistent storage of data for all processes. |
| **CSC Communications Task** | Performs encoding and decoding of data used during communications with the Ground Station. |
| **Inter System Communications Task** | Allows communications and data transfer with the payload computer. |
| **DTMF Task** | Receives and decodes command codes from the Ground Station. |
| **Development Terminal Task** | Developer interface used during development to debug processes. |

The central command task operates based on feedback from the System Control Task on what operating mode the satellite is required to be in. These operating modes are specified via two sources:

* Event triggers (such as hardware failure or low battery charge with no sunlight)
* DTMF Commands (nine digit codes to be transmitted from a Groundstation)

For more on the way in which DTMF is interpreted, see 6.4.1 DTMF

### Current Progress

All software drivers and applications compile and run as expected on the JTAG (LPC2119) boards. Each task has been written (with some clean up necessary) and tested to work individually, independent of the System Control Task.

The LPC2468 controller board has been designed, constructed and proofed. This board currently contains a USB interface to allow for quick programming. The board also currently has the capability to ‘hot swap’ three different kinds of memory modules. This allows for testing of the effectiveness of using different memory types for the purposes of implementing them on the satellite.

For all current drawings of the LPC2468, please consult the CRSC family of drawings.

### Future Work

All operating modes and DTMF commands need to be finalised and implemented. Currently, only examples of both functions exist. The focus so far has been on driver and low level application implementation. As such, currently all applications are run one at request of a user to facilitate module debugging. The Scheduler will need to be integrated System Control task to allow for the satellite to operate via specified operating modes.

Furthermore, the operating system and all applications and drivers need to be ported from the LPC2119 board to run on the LPC2468 board. Some settings and configurations need to be changed in order for drivers and applications to have the same functionality as on the JTAG boards. The code repository is also being refactored during this process to allow for a more formal and modular system.

The different memory types currently in tender also need to be tested and evaluated so that a final memory type can be chosen to be included on the final design.

Finally, the PCB for the LPC2468 CSC board needs to be finalised, with the USB interface removed and implementing the chosen memory type. This PCB needs to be designed such that it integrates with the other critical systems, sitting in Tray 2.

## Power Overview

The BLUEsat Power system is divided into three sub-systems, the Solar Array, the Battery Charge Regulator and Voltage Regulators.

The array will feed power into the Battery Charge Regulator which regulates power into the battery array. Power from this battery array then gets passed to the Voltage regulators, which distribute power to the different subsystems of the satellite. Figure 6.5 illustrates the flow of power from solar panels to each electrical subsystem in the satellite

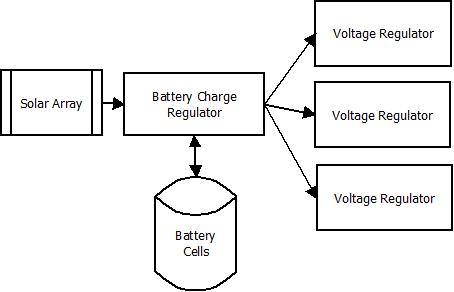


Figure 6.5 - Simplified overview of the Satellite Power System

The power system has been designed such that the Critical Systems computer is able to monitor and modify the state of the charging circuit, as well as being able to shut off power to different parts of the satellite.

## Solar Array

The current design for Solar Array consists of six solar panels. Each panel will sit 14 Gallium Arsenide solar cells connected in series. These six panels will sit on each of the six sides of the satellite, as illustrated in Figure 6.6.

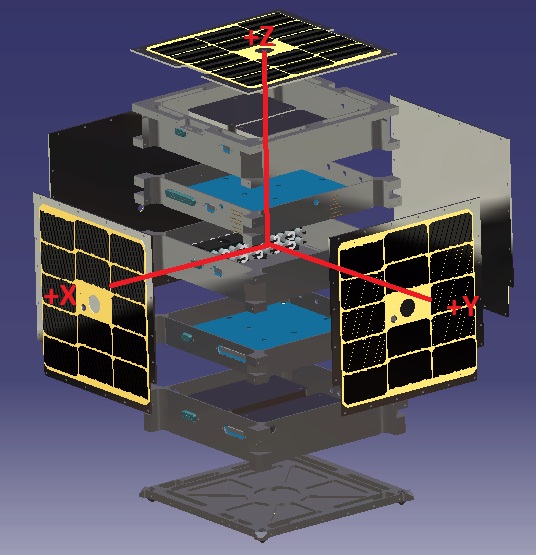


Figure 6.6 - Exploded view of Satellite structure including solar Array

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### Current Progress

BLUEsat currently has about 200 electrically functioning gallium arsenide solar cells and about 48 electrically non-functioning cells which are intended for use in mechanical testing. These cells are from Spectrolabs and are specifically designed for space, many being already used in space applications. These cells already have an inbuilt bypass diode and an anti-reflection coating for diffuse light.

These cells were purchased in 2004 and thus have undergone some degradation due to exposure to moisture and other factors. These cells have been kept in a clean room with desiccant in order to reduce the degradation due to moisture, some cells from the batch were tested recently and their efficiencies are relatively close to their data sheet efficiency of 21%. Theoretically we can still use these cells on the satellite if necessary providing that there enough cells in good operating condition

### Future Work

BLUEsat will need to obtain new cells from either via purchasing them outright or getting surplus from another project. The first method will require a large amount of capital so getting surplus cells would be preferable. Despite the fact it will help improve the performance of our satellite if surplus cell can’t be obtained and purchasing regular cells is too expensive the project will make do with the older cells.

If possible BLUEsat will obtain cells which already have their own cover glass in order to boost the overall efficiency and lifetime of the system. Before putting together the cells for the satellite’s solar panels members will have to undertake a course which teaches space grade soldering which will help ensure the panels last for the lifetime of the satellite.

## Battery Charge Regulator

*Relevant Drawings:*

|  |  |
| --- | --- |
| *POWR0001* | *BLUEsat Peak Power Tracker* |

BLUEsat will have four strings of eleven Nickel Metal Hydride (NiMh) battery cells, totalling a specified supply voltage of 13.2V.

Each battery string has a Battery Charge Regulator (BCR) sitting between it and the Solar Array Bus. The BCR serves two purposes: charging the battery, and ensuring maximum power is gained from the solar array.

The circuit itself is currently based upon the LT3652 Battery Charging Chip. Power to each BCR enters from the solar array bus, and is sent to the LT3652. This chip controls the peak power tracking, and battery charging, functionalities of the circuit. The circuit design can be found in drawing POWR001.

The LT3652 measures the current entering from the solar input over a 12 hour cycle, and adjusts a digital potentiometer such that the voltage across the solar input leads to maximum power into the battery.

Sensors also feed input into the LT3652, giving information about the battery temperature and power consumption. If the battery statistics are not within the required ranges, battery charging is stopped.

### Current Progress

The Battery Charge Regulator was implemented onto a prototype printed circuit board as part of William Du’s thesis on Peak Power Point Tracking (2011). However, when this circuit was recreated, it was found that batteries did not charge to full charge. This testing ended up damaging the current sample cells used in the project.

### Future Work

Currently the team is performing further testing on the performance of the PPT board and making modifications as necessary so that the BCR will perform to the standard required on the satellite.

In particular, the mechanism used to determine full charge on the batteries will need to be tested in greater detail. Once these issues are fixed, then the designs for the BCR can be finalised and integrated into the rest of the power system within the satellite.

## Voltage Regulation

## Telemetry

The satellite’s telemetry systems are designed to sense temperature and voltage at different points on the satellite. To this end the current telemetry system design allows for a network of up to 160 temperature and voltage sensors to feed data back to the critical systems computer. This data is then transmitted to Earth for analysis and action by Groundstation Operators.

The design of the Telemetry system is based around the MAX127 - an 8 channel Analogue to Digital converter. Each channel of the MAX127 is connected to either a voltage sampling point on the satellite or an amplified signal from a temperature sensor. Up to ten MAX127s can communicate on a single I2C serial line to the Critical systems computer. The system layout is illustrated in Figure 6.7.

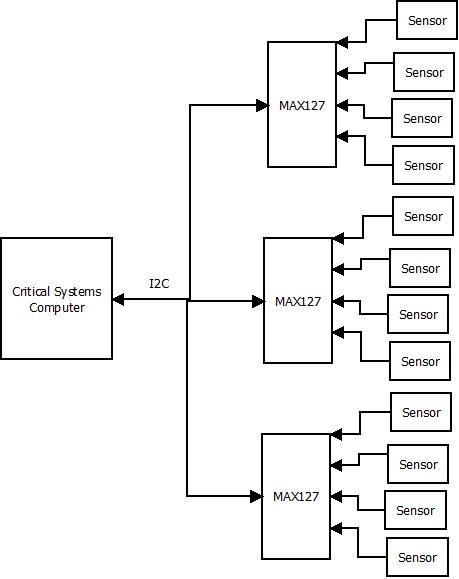


Figure 6.7 - Telemetry System Overview

### Temperature Sensors

The satellite utilises AD590 temperature sensors connected to a Current-Sense Amplifier. The AD590 outputs the current temperature in micro-amps, independent of voltage source. This current is amplified such that the MAX127 is able to take an accurate reading for analysis by the Critical Systems Computer.

For further detail on the Telemetry system and component circuitry, consult the TELM family of drawings.

### Current Progress

To date, the telemetry circuitry has been prototyped and proofed with accompanying software drivers. The current telemetry system is able to continuously poll and display the temperature of multiple sensors. All circuitry current sits on prototype Printed Circuit Boards with circuit schematics finalised according to the TELM family of drawings.

### Future Work

From current designs, the PCBs that will sit on the final satellite need to be designed. Telemetry ‘nodes’ need to be placed in each of the five trays of the satellite. Within each tray, each sensor will then have a local MAX127 ADC to communicate with. From the separate trays, PCBs will need to be designed such that the I2C communication lines from each MAX127 connect to the Critical Systems Computer on Tray 2.

Furthermore, the Telemetry software will need to be implemented such that it retains a history of data. Currently the Telemetry application is able to display information from the last poll, but is lacking functionality in being able to store previous telemetry information into the computer memory. The telemetry application will need to be extended so that it includes an effective memory storage system that will minimise the amount of space that a particular set of data will take.

## Payloads

### Payload Computer

### EDAC

### Namuru